having a passivation layer 32 as an upper surface thereof. An opening 34 is provided in the passivation layer 32 down to a bond or contact pad 36 of the semiconductor device 10. Any oxide that may be present on the upper surface of the contact pad 36 is removed by sputter cleaning. Fig. 2B illustrates the step of depositing an under bump metallurgy (UBM) 38 over the semiconductor wafer 30 and onto the contact pad 36. A photoresist layer 40 is deposited, developed and patterned to provide an opening 42 in the photoresist layer down to the UBM 38 overlying the contact pad 36 (Fig. 2C). As shown in Fig. 2D, a first electrically conductive material 44 is deposited into the opening 42 in the photoresist 40 and onto the UBM 38 overlying the contact pad 36. Ideally the first electrically conductive material 44 is deposited into the opening 42 in the photoresist layer 40 by electroplating. Preferably the first electrically conductive material includes solder, such as a 63 weight percent tin and 37 weight percent lead eutectic solder composition. A second electrically conductive material 46 is electroplated over the first electrically conductive material 44. Preferably the second electrically conductive material includes copper and nickel. The photoresist layer 40 is removed by ashing or etching (Fig. 2E). Thereafter, the excess UBM 38 is removed by etching or other suitable means (Fig. 2F). A flux agent 50 is then applied to the second electrically conductive material 46. The flux agent 50 may be applied by any of a variety of suitable means including brushing or spraying the flux agent 50 onto the second electrically conductive material 46 (Fig. 2 G). Examples of suitable flux agents may include, but are not limited to, compositions including boron oxide and phosphorus pentoxide. Thereafter, the semiconductor wafer with the first electrically conductive material 40, second electrically conductive material 46, and flux agent 50 is hard baked to

remove any oxide that may be on the surface of the second electrically conductive material 46 (Fig. 2H). The hard temperature typically is from about 120-140° C. Thereafter a portion of the semiconductor wafer 30 is dipped in an electroless plating solution 52 (Fig. 2I). Preferably, only the second electrically conductive material 46 is submerged in the electroless plating solution 52. The electroless plating solution 52 may include any of a variety of metals including copper, nickel, silver, and gold and mixtures thereof. The semiconductor wafer 30 is removed from the electroless plating solution 52 to provide a third electrically conductive material 54 deposited on the second electrically conductive material 46. Thereafter, the electrically conductive materials, 44, 46, 54 are reflown by heating the semiconductor wafer to form a bump 58 on the semiconductor wafer 30. The newly formed bump 58 has an improved height which is illustrated lines A-A in Fig. 2J. The method of the present invention improves the height of the bump by approximately 3-10 micrometers or approximately 10 percent over a standard solder bump that has been electroplated with copper and nickel.

[0067] Figs. 3A-F illustrates an alternative embodiment of a method of forming tall flip chip bumps according to the present invention. The alternative method utilizes the same steps as shown in Figs. 2A-D to provide a semiconductor wafer having a photoresist layer 40 deposited thereon with an opening therein down to the UBM 38 overlying a contact pad 36 of the semiconductor wafer 30. A first electrically conductive material 44 is deposited into the opening in the photoresist 40 and a second electrically conductive material 46 is electroplated over the first electrically conductive material 44 to provide the device shown in and described above with respect to Fig. 2D. Thereafter, a flux agent 50 is deposited over the second electrically

conductive material 46 as shown in Fig. 3A. Again, and the semiconductor device 30 is hard baked to remove any oxide that may be on the surface of the second electrically conductive material 46 (Fig. 3B). The hard bake temperature ranges from about 120-140° C. Because the photoresist layer 40 is still present over the semiconductor wafer 38, the hard baking step makes the subsequent removal of the photoresist layer more difficult. However, leaving the photoresist on during the hard bake results in a more uniform height of the bumps on the wafer. Alternatively, with the photoresist layer 40 still on the semiconductor wafer 30, the semiconductor wafer may be soft baked at a temperature ranging from about 90-100° C to remove any oxide on a second electrically conductive material 46. The photoresist layer 40 is removed by etching as shown in Fig. 3C and any excess UBM 38 is also removed by etching. A portion of the semiconductor wafer 30 is dipped in an electroplating solution 52 in the same manner as indicated in the other embodiment of the invention (Fig. 3G). The semiconductor wafer 30 is removed from the electroless plating solution 52 to provide a third electrically conductive material 54 deposited on a second electrically conductive material 46. The electrically conductive materials 44, 46 and 54 are heated to reflow the same and form a bump 58 of improved height on the semiconductor wafer 30. Again, an increase in bump height of about 3-10 micrometers or 10 percent is accomplished according to the present invention as indicated by arrows A-A in Fig. 3F.